100G ER1 BIDI Transceiver

The 100G ER1 BIDI Optical Transceiver module **ACT-EQ28-ER1C-XXXX-Y** is an optical transceiver module designed for single channel O-band up to 40km optical transmissions. The module converts 4x25Gb/s NRZ electrical input data to single channel optical signals for 100Gb/s optical transmission, Reversely, on the receiver side, the module optically converts a 100Gb/s optical input data to 4x25Gb/s NRZ electrical output data.

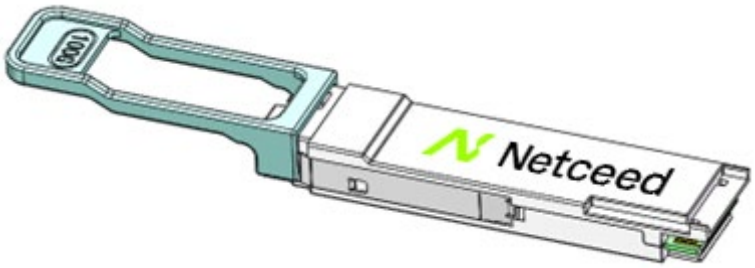
The optical interface of the module is a simplex LC and is compliant to the QSFP28 MSA, 100G Lambda MSA.It provides an excellent solution for 100G data transmission up to 40km single mode fiber.

FEATURES

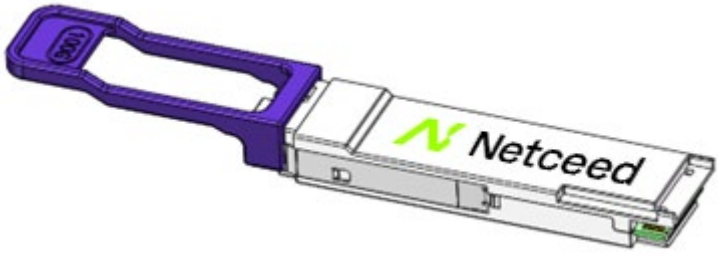
- Hot-pluggable QSFP28 form factor
- Support Ethernet CAUI-4
- High Sensitivity APD Receiver
- Operation case temperature C-Temp
- Single 3.3V power supply
- Aligned with IEEE 802.3bs and 100G Lambda MSA
- Simplex LC receptacles
- I2C management interface
- RoHS-6 compliant

APPLICATIONS

- Transmission up to 40km
- Ethernet



UP-LINK



DOWN-LINK

ORDERING INFORMATION

PN	Operation Temperature	Support Rate	Description
ACT-EQ28-ER1C-3031-H	0C~70C	CAUI-4	QSFP28 100G BIDI,40km,C-Temp,Support Ethernet,Up-link.
ACT-EQ28-ER1C-3030-H	0C~70C	CAUI-4	QSFP28 100G BIDI,40km,C-Temp,Support Ethernet,Down-link.

SCHEMATIC DIAGRAM

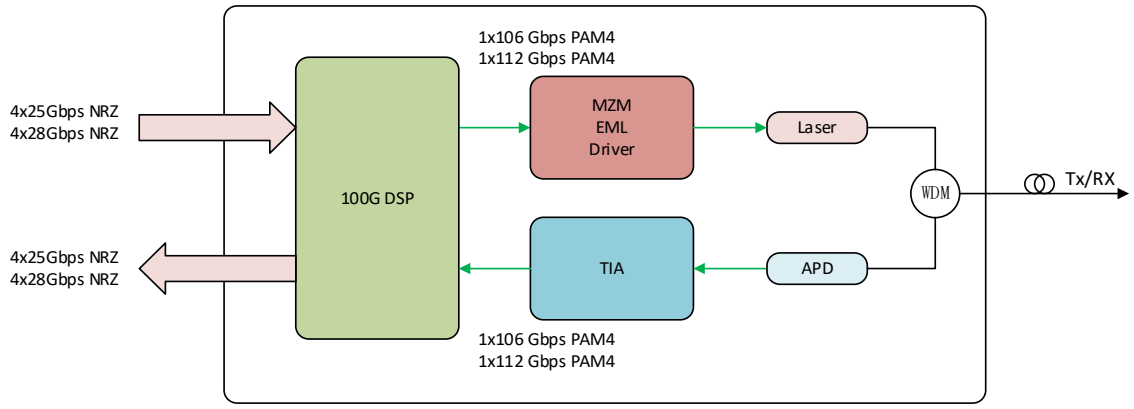


Figure 1: Block Diagram

ABSOLUTE MAXIMUM RATINGS

Table 1: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Maximum Supply Voltage	Vcc	0	3.6	V	
Storage Temperature	Ts	-40	85	℃	
Relative Humidity (no-condensation)	RH	0	85	%	
Damage Threshold	THd	-2.4		dBm	

RECOMMENDED OPERATING CONDITIONS

Table 2: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc		1.2	1.36	A	
Power Consumption			4	4.5	W	
Case Temperature	C-Temp	0		70	℃	
Link Distance	D			40	km	

KEY SPECIFICATIONS

Table 3: Transmitter Optical Specifications, EOL

Parameter	Symbol	Min	Typ	Max	Unit
Data Rate (each Lane)		53.125 ± 100 ppm(CAUI-4)			GBd
Modulation Format		PAM4			
Wavelength	UP-LINK	1304.58+/-1.0			nm
	DOWN-LINK	1309.14+/-1.0			
Side-mode Suppression ratio	SMSR	30			dB
Average launch power[1]	P_{AVG}	1.7		7.1	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) TECQ<1.4dB TECQ>1.4dB	P_{OMA}	 4.7 3.3+TECQ		7.9	dBm
Transmitter and Dispersion penalty	TDECQ			3.9	dB
TECQ	TECQ			3.9	dB
|TDECQ-TECQ|（max）				2.7	dB
Extinction Ratio		5.0			dB
Optical Return Loss Tolerance				15	dB
Transmitter Reflectance[2]	RL			-26	dB
Average Launch Power OFF Transmitter	P_{off}			-15	dBm
$RIN_{15.6}$ OMA	RIN			-136	dB/Hz

Notes:

1. Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter Reflectance is defined looking into the transmitter.

Table 4: Receiver Optical Specifications, EOL

Parameter	Symbol	Min	Typ	Max	Unit
Data Rate (each Lane)		53.125 ± 100 ppm(CAUI-4)			GBd
Modulation Format		PAM4			
Lane Wavelength	UP-LINK	1309.14+/-1.0			nm
	DOWN-LINK	1304.58+/-1.0			
Damage Threshold[1]		-2.4			dBm
Average receive power[2]		-16		-3.4	dBm
Receive Power (OMA_{outer})				-2.6	dBm
Receiver Reflectance				-26	dB
Receiver sensitivity (OMAouter)[3]				Max(-13.8, TECQ-15.2)	dBm
Stressed receiver sensitivity (OMAouter), each laned (max)[4]	SRS			-10	dBm
Transmitter Reflectance				-26	dB
LOS Assert	LOSA	-30		-19.5	dBm
LOS De-assert	LOSD			-16.5	dBm
LOS Hysteresis	LOSH	0.5			dB
Conditions of Stress Receiver Sensitivity Test					
Stressed eye closure for PAM4 (SECQ), lane under test				3.9	dB

Notes:

1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane.
2. Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. CAUI4 mode,the Pre-FEC BER level is 2E-4.
4. Measured with conformance test signal at TP3 for the BER specified in IEEE Std 802.3cd.

Table 5: Transmitter High Speed Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Signaling rate	*Rate*	25.78 (CAUI-4)			Gbps
Differential Input Impedance	Z_d	-	100	-	Ω
Differential Input Voltage per lane	-	-	-	900	mV
Input impedance mismatch	-	-	-	10	%
Input High Voltage	*VIH*	2	-	V_{cc}+0.3	V
Input LOW Voltage	*VIL*	-0.3	-	0.8	V

Table 6: Receiver High Speed Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Signaling rate	*Rate*	25.78 (CAUI-4)			Gbps
Common mode voltage	*Vcm*	-350	-	2850	mV
Common Mode Noise, rms	-	-	-	17.5	mV
Differential Termination Resistance Mismatch (at 1 MHz)	-	-	-	10	%
Differential Return Loss (SDD22)	-	-	-	Per CEI-28G-VSR	dB
Common Mode to Differential conversion and Differential to Common Mode Conversion (SDC22, SCD22)	-	-	-	Per CEI-28G-VSR	dB
Common Mode Return Loss (SCC22) - from 250 MHz to 30 GHz	-	-	-	-2	-
Transition Time: 20/80%	-	9.5	-	-	ps
Vertical Eye Closure	*VEC*	-	-	6.5	dB
Eye width at 10-15robability	*EW15*	0.57	-	-	UI
Eye height at 10-15 probability	*EH15*	228	-	-	mV

MOUDLE CONNECTOR PAD LAYOUT

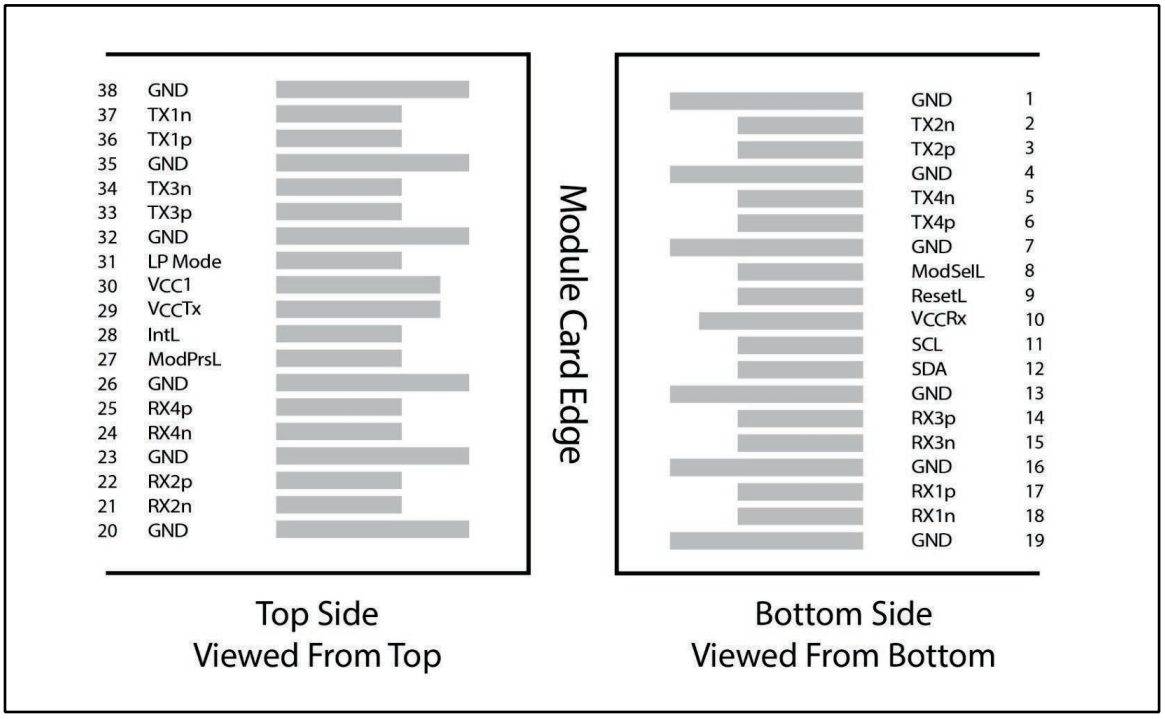


Figure 2: QSFP28 Connector Pad layout

Table 7: Module Connector Pad Definition

PIN	Logic	Symbol	Name / Description
1	GND	*GND*	Ground
2	CML	*Tx2n*	Transmitter Inverted Data Input
3	CML	*Tx2p*	Transmitter Non-Inverted Data Input
4	GND	*GND*	Ground
5	CML	*Tx4n*	Transmitter Inverted Data Input
6	CML	*Tx4p*	Transmitter Non-Inverted Data Input
7	GND	*GND*	Ground
8	LVTTL	*ModSelL*	Module Select
9	LVTTL	*ResetL*	Module Reset
10	VCC	*VCC_Rx*	+3.3V Receiver Power Supply
11	LVCMOS	*SCL*	2-wire Serial Interface Clock
12	LVCMOS	*SDA*	2-wire Serial Interface Data
13	GND	*GND*	Ground
14	CML	*Rx3p*	Receiver Non-Inverted Data Output
15	CML	*Rx3n*	Receiver Inverted Data Output
16	GND	*GND*	Ground
17	CML	*Rx1p*	Receiver Non-Inverted Data Output

18	CML	*Rx1n*	Receiver Inverted Data Output
19	GND	*GND*	Ground
20	GND	*GND*	Ground
21	CML	*Rx2n*	Receiver Inverted Data Output
22	CML	*Rx2p*	Receiver Non-Inverted Data Output
23	GND	*GND*	Ground
24	CML	*Rx4n*	Receiver Inverted Data Output
25	CML	*Rx4p*	Receiver Non-Inverted Data Output
26	GND	*GND*	Ground
27	LVTTL	*ModPrsL*	Module Present, grounded inside the module
28	LVTTL	*IntL*	Interrupt
29	VCC	*VCC_Tx*	+3.3V Transmitter Power Supply
30	VCC	*VCC1*	+3.3V Power Supply
31	LVTTL	*LPMode*	Low Power Mode, active high
32	GND	*GND*	Ground
33	CML	*Tx3p*	Transmitter Non-Inverted Data Input
34	CML	*Tx3n*	Transmitter Inverted Data Input
35	GND	*GND*	Ground
36	CML	*Tx1p*	Transmitter Non-Inverted Data Input
37	CML	*Tx1n*	Transmitter Inverted Data Input
38	GND	*GND*	Ground

FUNCTIONAL DESCRIPTION

Electrical interface: All signal interfaces are compliant with the QSFP28 MSA specifications. The high speed DATA interface is differential AC-coupled internally and can be directly connected to a 3.3V SERDES IC. Hardware control and status reporting pins include a 2-wire serial interface (SCL and SDA) and five 3.3V LVTTL hardware signals (ModSelL, ResetL, LPMode, ModPrsL, and IntL). The 2-wire interface pins are 3.3V LVCOMS compatible. Hosts shall use pull-up resistor connected to Vcc_host on each of the 2-wire interface SCL, SDA, and all low speed status outputs.

ModSelL: The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected.

Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL: The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode: The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, and Power_set software control bits (Address A0h, byte 93 bits 0,1), the host controls how much power a module can dissipate. The allowed QSFP28 power consumption is shown in below truth table.

LPMode PIN State	Power_ override bit	Power_ set bit	Power Allowed
1	0	X	1.5W
0	0	X	4W
X	1	1	1.5W
X	1	0	4W

ModPrsL: ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL: IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read
(see SFF-8636).

INTERACING THE TRANSCEIVER

Host can determine the characteristic and status of the transceiver through a 2-wire common management interface. The interface also provides host a mechanism to control the operation of a module. SFF-8636 describes the interface details such as memory map and communication protocol used to transfer information between host and a module.

The common memory map is arranged into a single lower page address space (A0h) of 128 bytes and multiple upper address pages. This structure permits timely access to addresses in the lower page such as interrupt flags and monitors. Less time critical entries such as serial ID information and threshold settings are available with the page select function.

DIGITAL DIAGNOSTIC MEMORY MAP

Table 8: Lower Memory Overview

Address	Size	Subject Area	Description
0–3	4	ID and Status Area	Module ID from SFF-8024 list, version number, Type and status
			Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4–7	4	Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh
8–13	6	Module-Level Flags	All flags that are not lane or data path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or data path specific
26-30	5	Module Global Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Flag Masks	Masking bits for the Module-Level flags
37-38	2	CDB Status Area	Status of most recent CDB command
39-40	2	Module Firmware Version	Module Firmware Version.
41-63	23	Reserved Area	Reserved for future standardization
64-82	19	Custom Area	Vendor or module type specific use
83-84	2	Inactive Firmware Version	Version Number of Inactive Firmware. Values of 00h indicates module supports only a single image.
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s)
118-125	8	Password Entry and Change	
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page

MECHANICAL DIMENSIONS

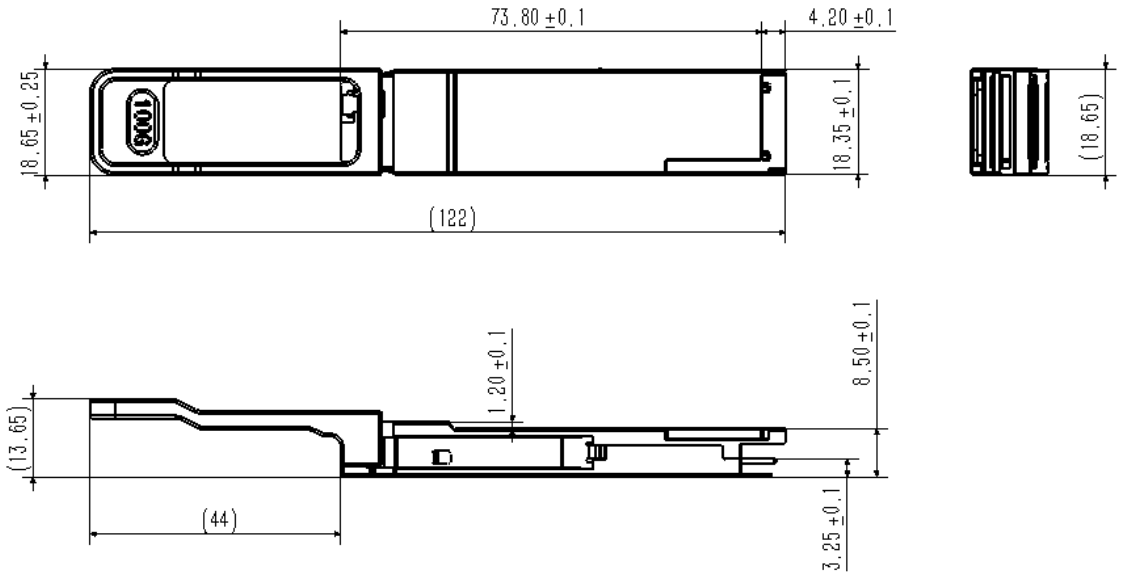


Figure 4: Mechanical Schematic

DIGITAL DIAGNOSTIC

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Table 9: Digital Diagnostic

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-3	3	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-3	3	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

LASER SAFETY

This is a Class 1 Laser Product according to EN/IEC 60825-1:2014. This product Complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019. Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.